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09/733,401	12/08/2000	James Murray	003242.P014	1880

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EXAMINER	
SCHNEIDER, JOSHUA D	
ART UNIT	**PAPER NUMBER**
2182	13

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/733,401	Applicant(s) MURRAY ET AL.	
	Examiner Joshua D Schneider	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6,12-16 and 21-32* is/are pending in the application.

4a) Of the above claim(s) *23 and 28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,12-16, 21,22,24-27,and 29-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 3/1/2004 have been fully considered but they are not persuasive. The Kamiya reference is used to teach the termination and re-execution of a DMA transfer. The applicant has argued that the termination and re-execution of the transfer of Kamiya is not the same as that taught by the applicant. Applicant has concluded that the interruption and resumption is not equivalent to the termination of a DMA transfer. While this may be true, this is not what is taught by Kamiya. It is quite clear from the reference that the transfer is terminated, and that only after an entirely different second DMA transfer is completed that the first transfer is restarted.

2. The suspension of operations to which applicant refers is well known, and is quite different from the operation of Kamiya. U.S. Patent 6,199,121 to Olsen et al. explains one such interruption and resumption caused by polling in chained burst transfers (see Background of the Invention). . With regards to claim 1, the termination of the current transfer operation is undeniable. While Kamiya teaches a more robust system that does not have to resend all of the blocks that have been correctly completed, is certainly still teaches the interruption of a transfer. Likewise, with regards to claims 12, 13, and 15, the restarting of the operations saved in the backup channels of this controller also must be a retransmission as claimed, as whatever block that was terminated before the terminal count was reached must be retransmitted to be completed correctly. While the applicant requires only a system without such backup control abilities, Kamiya does teach termination and retransferring over DMA channels.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 6, 12-16, 21 and 24-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,809,335 to Kamiya in further view of the applicant admitted prior art (AAPA). With regards to claim 1, Kamiya teaches a direct memory access (DMA) controller (Fig. 2, element 13, of Fig. 1, element 1, and column 3, lines 45-54), external modules (Fig. 1, elements 4, 6, and 8), and the termination of a DMA transfer before a terminal count is reached (column 8, lines 30-41). The reception of a high priority request by this controller is a signal to terminate the current transfer and start the high priority transfer. Kamiya does not explicitly teach the external modules being I/O devices, but this is taught to be well known by the AAPA (page 2, lines 13-18). It would have been obvious to one of ordinary skill in the art at the time of invention to combine the termination of Kamiya with the I/O devices of the AAPA to create a system that is compatible with known device types and competitive in a modern computer marketplace.

5. With regards to claim 2, Kamiya teaches the re-execution of a DMA transfer (column 8, lines 47-50) with an I/O device (external module). The signaling of the end of a high priority request by this controller is a signal to re-execute the terminated transfer.

6. With regards to claim 6, Kamiya teaches a system interconnect (Fig. 1, element 1), coupled to the I/O device (external modules, Fig. 1, elements 6 and 8) and a DMA controller

(Fig. 2, element 13, of Fig. 1, element 1), a CPU coupled to the system interconnect (Fig. 1 elements 3 and 1), and a external modules coupled to the system interconnect (Fig. 1, elements 4, 6, and 8). It would have been obvious to one of ordinary skill in the art at the time of invention that the one of the external modules would have to be a memory device in order for the DMA transfer to be a memory access, as defined.

7. With regards to claim 12, Kamiya teaches a direct memory access (DMA) controller (Fig. 2, element 13, of Fig. 1, element 1, and column 3, lines 45-54), external modules (Fig. 1, elements 4, 6, and 8), and the termination of a DMA transfer (column 8, lines 30-41). Kamiya does not explicitly teach the external modules being I/O devices, though this is taught to be well known by the AAPA (page 2, lines 13-18). Kamiya teaches the re-execution of a DMA transfer (column 8, lines 47-50) with an I/O device (external module).

8. With regards to claims 13 and 15, Kamiya teaches a direct memory access (DMA) controller to transfer data between and first and second device (Fig. 2, element 13, of Fig. 1, element 1, and column 3, lines 45-54), external modules (Fig. 1, elements 4, 6, and 8), and the termination of a DMA transfer before a terminal count is reached (column 8, lines 30-41). The reception of a high priority request by this controller is a signal to terminate the current transfer and start the high priority transfer. Kamiya does not explicitly teach the external modules being I/O devices, though this is taught to be well known by the AAPA (page 2, lines 13-18). Kamiya teaches the termination of a DMA transfer (column 8, lines 30-41) with an I/O device (external module). Kamiya teaches the re-execution of a DMA transfer (column 8, lines 47-50) with an I/O device (external module). The signaling of the end of a high priority request by this controller is a signal to re-execute the terminated transfer. The use of acknowledge signals is not

explicitly taught by Kamiya. However, the AAPA teaches that it is well known to use acknowledge signals to acknowledge control signal from an I/O device (page 2, lines 13-18). It would have been obvious to one of ordinary skill in the art at the time of invention, to use the well known request and acknowledge control signal lines of the AAPA with the termination and re-execution of Kamiya to create a system which can terminate and re-start DMA transfers, in order to provide a more robust I/O system which can handle CPU interrupts without causing fatal errors in a transfer currently being processed, and will provide greater system stability.

9. With regards to claim 14, Kamiya teaches the reloading the configuration registers with control information (column 8, lines 43-46). It is inherent that this reloading would take place before the transmission of an acknowledge signal which would occur during the following restarting process.

10. With regards to claim 16, Kamiya teaches the reloading the configuration registers with control information (column 8, lines 43-46). It is inherent that this reloading would include the clearing of a well known transfer size counter within the DMA controller that would occur before the following restarting process of the DMA block transfers and the acknowledge signal to the first device to start the transfer.

11. With regards to claim 21, Kamiya teaches the re-execution of a DMA transfer (column 8, lines 47-50) with an I/O device (external module). The signaling of the end of a high priority request by this controller is a signal to re-execute the terminated transfer. The use of acknowledge signals is not explicitly taught by Kamiya. However, the AAPA teaches that it is well known to use acknowledge signals to acknowledge control signal from an I/O device (page 2, lines 13-18).

12. With regards to claims 24 and 29, Kamiya teaches a first channel coupled to the I/O device to facilitate the transfer of data (Fig. 2).

13. With regards to claims 25 and 30, Kamiya teaches memory means to store configuration data (Fig. 2). While Kamiya does not call this memory registers, the use of registers in DMA controllers is well known.

14. With regards to claims 26 and 31, error-checking logic is well known in the art for checking data transfers for errors.

15. With regards to claim 27, Kamiya teaches control logic to control the transfer of the data (Fig. 2, element 13)

16. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,809,335 to Kamiya and the applicant admitted prior art (AAPA) as applied to claims 1, 2, 6, 12-16, 21 and 24-32 above, and further in view of U.S. Patent 5,903,775 to Murray.

17. With regards to claim 22, Kamiya teaches the re-execution of a DMA transfer (column 8, lines 47-50) with an I/O device (external module). The signaling of the end of a high priority request by this controller is a signal to re-execute the terminated transfer. The use of acknowledge signals is not explicitly taught by Kamiya. However, the AAPA teaches that it is well known to use acknowledge signals to acknowledge control signal from an I/O device (page 2, lines 13-18). Kamiya and the AAPA do not explicitly teach the use of a system to terminate a data transfer and to restart the same transfer. Murray teaches and error-checking system that upon the occurrence of an error terminates the transfer through the use of interrupts (column 12, lines 40-56). The interrupt handler retransmits the data that has not been properly transmitted (column 12, line 12, through column 14, line 18). It would have been obvious to one of ordinary

skill in the art at the time of invention to combine the termination and re-execution of Kamiya with the error handling of Murray in order to eliminate data loss from transfer errors and increase functionality.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 6,192,492 to Masiewicz et al. teaches the suspension and resumption of DMA transfers. U.S. Patent 6,199,121 to Olson et al. teaches the suspension and resumption of DMA transfers.

19. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however,

will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua D Schneider whose telephone number is (703) 305-7991. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDS

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